caeleste

Charge domain binning by applying potentials between photodiodes

<u>S. Boulanger¹</u>, A. Kalgi¹, B. Dierickx¹, B. Sezgin¹, D. Gautam¹, B. Van Camp¹, Y. Creten¹, J. Vermeiren¹, Shirly Regev², K. Minoglou³

¹ Caeleste – Hendrik Consciencestraat 1b – 2800 Mechelen, Belgium

² Etesian – Ha-Oren St 5 – Ramat Yishay, Israel

³ ESA-ESTEC – Keplerlaan 1, 2201 AZ Noordwijk, The Netherlands

Outline



Binning

- Charge domain binning
- TCAD simulations of charge binning concept
- Measurement results of sensor with charge binning
- Conclusions

Binning



- In image sensors, for low illumination levels, the photogenerated charges of multiple pixels are combined to improve SNR
 - E.g., In 2x2 pixel binning, we ideally have
 - 4 times more signal per "2x2 pixel"
 - 2 times higher SNR if photon shot noise limited ($\sigma_{PSN}^2 = 4 \cdot N_{e^-} \cdot q$)
 - However, spatial resolution is divided by 4
- There are 2 ways to accomplish binning
 - Voltage domain binning
 - Averaging 4 pixels in the voltage domain
 - Relatively easy to do, read noise is included in the averaging
 - Charge domain binning
 - All photogenerated charges are integrated only in a single pixel

Binning



- Charge domain binning
 - Signal is amplified at the earliest stage resulting in lower input referred noise
 - Challenges
 - Modulation of the electric field is required
 - Potentially increased dark current, try to avoid regions with trap states
 - Try to avoid "dead zones" where electrons and holes might recombine



23/06/2023

Charge binning – TCAD

- We perform 2D TCAD simulations
 - Look at multiple EPI layer thicknesses
 - Uniform light (400nm) on the backside
 - Reference situation
 - What is the total available photocurrent in unbinned operation?
 - Is the EPI layer Fully depleted?
 - Binning situation
 - What is the total collected photocurrent?
 - Is there recombination?
 - Look at depletion regions
 - Extra:
 - Can we apply a voltage on the backside?





Caeleste Confidential

caeleste

TCAD – Reference situation

caeleste

- Normal operating pixel
 - All pixel photodiodes are tied to $V_{dep} = 1V$
 - EPI thickness is 10μm
- Probe photocurrent through photodiode contacts
 - The total light to that can be collected using charge binning in total should be 2X these numbers



Pitch [µm]	Photocurrent per pixel [<i>pA</i> /μ <i>m</i>]
7.5	1.1
9.5	1.4
15	2.2

Photocurrents for $10\mu m$ EPI thickness, $V_{on} = 1V$

TCAD – Binning situation

- Modulation of the electric field by asymmetrical expansion of the depletion region is possible
- One pixel at $V_{dep} = 1V$, the other is at $V_{off} = 0V$
- Probe photocurrent through the collecting and non-collecting photodiode





23/06/2023

TCAD – Recombination

caeleste



This means limited recombination

Pitch [µm]	Total avail. photocurrent [<i>pA/μm</i>]	Collecting [pA/μm]	Off [pA/μm]	Total collecting + off [$pA/\mu m$]
7.5	2.2	10.0	-7.9	2.1
9.5	2.8	2.0	0.8	2.8
15	4.4	2.8	1.5	4.3

(Photo)currents for $10\mu m$ EPI thickness, $V_{on} = 1V$, $V_{off} = 0V$



23/06/2023

Caeleste Confidential

Pitch [µm]	Total avail. photocurrent [<i>pA/μm</i>]	Collecting [pA/μm]	Off [pA/μm]	Total collecting + off [<i>pA/μm</i>]
7.5	2.2	10.0	-7.9	2.1
9.5	2.8	2.0	0.8	2.8
15	4.4	2.8	1.5	4.3

Leakage↑ if smaller pitch/p-well widths

Leakage↑ if larger V differences on PDs

Will appear in the image as dark current

Further investigation yielded:

Leakage↑ if thicker EPI

TCAD – Leakage





9

TCAD – EPI thickness



2D TCAD setup – doping profile (colors) and depletion region (white lines) 10

Caeleste Confidential

As pixel pitch grows larger than the **EPI thickness**, the modulation depth becomes smaller

- Electrons have to diffuse in weak electric fields
- Thicker EPI also means that it is harder to achieve full depletion

EPI [μm]	Total avail. photocurrent [<i>pA</i> /μm]	Collecting [pA/μm]	Off [pA/μm]	Total collecting + off [$pA/\mu m$]
10	4.4	2.8	1.5	4.3
23	3.3	2.8	0.5	3.3

(Photo)currents for $15\mu m$ pitch, $V_{dep} = 1V$, $V_{off} = 0V$

3

TCAD – Backside voltage

caeleste

- Applying a backside biasing voltage to …
 - Extend depletion regions towards the backside, and
 - Increase the electric field strength such that electrons are not diffusing



2D TCAD setup for EPI thickness $23\mu m$, $V_{on} = 2V$, $V_{off} = 0V$ – Electrostatic potential (colors and black lines) and depletion region (white lines)

TCAD – Backside voltage



- Applying a backside biasing voltage will result in a majority carrier current (hole current)
 - Current flows from pixel substrate to backside surface P+ layer (P+/P--/P+ junctions)
 - It means a significant DC current per pixel



Pitch [<i>µm</i>]	Total avail. photocurrent [<i>pA</i> /μm]	Backside voltage [<i>V</i>]	Collecting [<i>pA/μm</i>]	Off [pA/μm]	Collecting + off [<i>pA</i> /μm]	Hole current [<i>nA/μm</i>]
15	3.3	0	5.8	-2.6	3.2	0
15	3.3	-1	2.6	0.7	3.2	2.2
15	3.3	-2	3.4	1.0	4.4	14
15	3.3	-3	2.3	1.1	3.4	36
15	3.3	-5	2.1	1.2	3.3	110

(Photo)currents for $23\mu m$ EPI thickness, different backside voltages, $V_{on} = 2V$, $V_{off} = 0V$

• Curiously, this results in some photo-gain for $V_{backside} = -2V$

Charge binning – TCAD – Backside voltage

Majority carrier current



caeleste

Project

caeleste

- ELFIS2
 - Backside illumination (BSI)
 - High QE at near-infrared wavelengths
 - TID and SEL/SEU radiation-hard design
 - "True", Motion-Artifact Free (MAF), High Dynamic Range (HDR)
 - Reads same photogenerated charges on two different conversion capacitances
 - Full dynamic range for single integration time
 - Integrate-While-Read (IWR) Global Shutter (GS) CMOS technology, allowing
 - Low noise readout using Correlated Double Sampling (CDS)
 - Global shutter without dark current penalty
 - Goal:
 - Binning in charge domain



ELFIS2 is the successor of ELFIS Dierickx & al,"A rad-hard, global shutter, true HDR, backside illuminated image sensor", Space & Scientific CMOS Image Sensors Workshop, Toulouse, 26-27 Nov 2019

Charge binning implementation



VDDpix

VDDpix

VDDpix

- Charge domain binning gathers all photogenerated charges into a single pixel
 - "Turn off" surrounding pixels by tying the PPD to 0V



Charge binning measurements



- Implemented on ELFIS2
 - Ideal: 4X higher curve
 - Actual: 2X higher response curve
 - $15\mu m$ pitch
 - 22µm EPI thickness
 - 1/4 pixels are fixed at 0.1V
 - $V_{dep} = \sim 0.1 V$





Caeleste Confidential

23/06/2023

Conclusions



- We performed TCAD simulations for enabling charge binning
 - Electric field can be changed applying potentials
 - Applying a backside potential also causes a DC current from PWELL to backside
 - EPI layer thickness and size of the P-WELLs for transistors are critical
 - Leakage current was observed, which can cause an increase in dark current
- We have implemented charge binning on ELFIS2
 - A factor 2 gain improvement was achieved
 - The low depletion voltage $V_{dep} \sim 0.1V$ was the main limitation
 - Backside biasing was not possible due to limited conductivity in the backside passivation layers
- Future improvements
 - Avoid low depletion voltages
 - Avoid applying a voltage
 - Disable TG/TG2 for odd columns (not just the rows)
 - Process optimization to be able to have full lateral depletion and low resistivity back side p+ implant.



THANK YOU

HDR operation to charge binning

- HDR allows us to extend the range on the "high signal" side
- What about the "low signal" side?
 - Perhaps we can trade of pixel area for SNR?
 - Binning!





2

2

4

4

Project ELFIS2

- Specifications (measured)
- Other properties
 - Stitched design
 - Region Of Interest in Y-direction
 - Fixed Pattern Noise reduction
 - Voltage domain binning
 - Charge domain binning
 - Low noise mode
 - High-resistive epitaxial layer
 - Back-side illumination
 - Back-bias capability
 - Analog outputs

Specification	Value
Stitch block size	1024 x 512
Possible resolutions	1024 x 512, 2048 x 2048 , 9k x 9k
High-gain full well	13 <i>ke</i> -
Low-gain full well, integrate-while-read	$180ke^-$
Low gain full well, integrate-then-read	360ke ⁻
Region of interest in Y	
Read noise (nominal, global shutter)	$3.5e_{RMS}^{-}$
EPI thickness	6.5μm, 12μm, 22μm
Quantum efficiency ($22\mu m$ EPI)	~80%@400nm, ~85%@540-700nm, ~30%@1000nm
MTF ($12\mu m$ EPI)	0.52
PLS	1/4000@630nm, 1/600@830nm
Image lag	<0.5%
PPD dark current	< 500 <i>e</i> ⁻ / <i>s</i>
Output channels (2k x 2k)	16
Nominal channel rate	40MHz
Frame rate (2k x 2k)	150fps

ELFIS2 operation

caeleste

- During integration
 - Charges overflow from PPD to C_a through TG_{3a}
- Global operation
 - PPD to SN through *TG*₁
 - PPD to C_a through TG_{3a} to transfer remaining charges
- Readout
 - High-gain: SN to FD through *TG*₂
 - Low-gain: Averaging of FD and C_a



HDR operation



- During integration
 - Excess of charges can overflow from PPD to the extra capacitor C_a
 - Apply a voltage to TG3a to control for how much photogenerated charge the overflow starts to happen



HDR operation



- During readout
 - Step 1: transfer all the remaining charges from PPD to the storage node SN.
 - Step 2: after reading the reset, transfer those charges from SN to the floating diffusion FD.
 - Step 3: after reading the signal, short the switches to read the voltage on C_a .

